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(54) Method of manufacturing a semiconductor wafer comprising a dopant evaporation preventive film on one main surface and an epitaxial layer on the other main surface

(57) There is disclosed a method of manufacturing a semiconductor wafer which has a dopant evaporation preventive film formed on one of main surfaces thereof, wherein a film serving as the dopant evaporation preventive film 2 is formed on the one of the main surfaces by a plasma CVD method. There is also disclosed a method of manufacturing a semiconductor wafer having a plasma CVD film 5 on one of main surfaces, wherein the plasma CVD film 5 is formed on the one of the main surfaces of the semiconductor wafer 4 so that a stress between the plasma CVD film 5 and the semiconductor wafer 4 falls in a range of 1×10^8 - 1×10^9 dyne/cm^2.

FIG. 1A

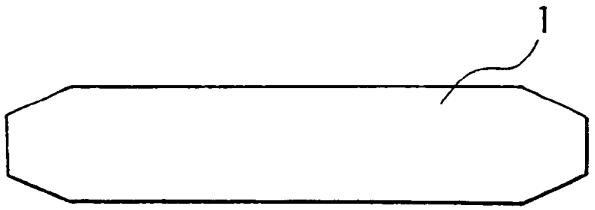

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FIG. 1B

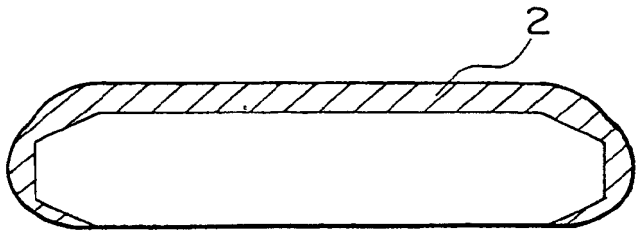


FIG. 1C

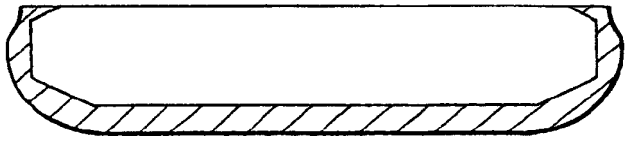
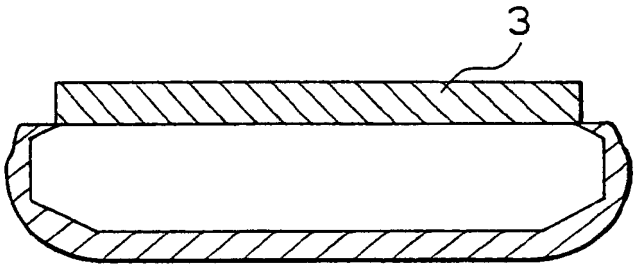


FIG. 1D



Description

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to a method of manufacturing a semiconductor wafer and a semiconductor wafer manufactured by the method, and particularly to a method of manufacturing a semiconductor wafer having a film formed through plasma chemical vapor deposition (hereinafter referred to as plasma CVD) and a semiconductor wafer manufactured by the method. Further, the present invention relates to a semiconductor epitaxial wafer, or a semiconductor wafer on which an epitaxial layer is grown, and a method of manufacturing the same.

Description of the Related Art:

In an epitaxial growth process wherein a thin monocrystalline silicon film is grown on a silicon wafer in gas phase, the silicon wafer is usually exposed to a high temperature of not less than 1000°C. During this process, a dopant evaporated from the silicon wafer is incorporated into a growing epitaxial layer through a gas phase. This phenomenon is typically termed autodoping. When autodoping is prominent, an epitaxial layer having a desired resistivity cannot be obtained. Consequently, a semiconductor element having this epitaxial layer becomes defective due to a failure to exhibit designed characteristics.

Autodoping becomes prominent when the resistivity of a silicon wafer is relatively low. Therefore, according to a generally employed method, when an epitaxial layer is formed on a wafer having a relatively low resistivity, a silicon oxide film (hereinafter abbreviated to an "oxide film"), serving as a film that prevents autodoping (a dopant evaporation preventive film), is formed on one of the main surfaces of a silicon wafer (hereinafter referred to as a "back surface") on which no epitaxial layer is grown.

A conventionally used oxide film to be formed on the back surface is:

1) an atmospheric pressure chemical vapor deposition (atmospheric pressure CVD) oxide film grown in an atmospheric pressure CVD system, or
2) a thermal oxide film grown through oxidation within a heat treatment furnace.

However, either of the oxide films causes a relatively large stress to a silicon wafer, resulting in a potential warpage of the silicon wafer or crystal defects in the silicon wafer. Furthermore, in the case of a thermal oxide film, since a dopant doped in a silicon wafer is incorporated into the thermal oxide film during the formation of the thermal oxide film, autodoping occurs due to dopant being released from the thermal oxide film during a subsequent epitaxial growth process. Therefore, the thermal oxide film fails to properly function as a film that prevents autodoping.

In addition, when either of the oxide films is formed, the oxide film is formed not only on the back surface of a silicon wafer but also on the other main surface (hereinafter referred to as a "front surface") on which an epitaxial layer is grown. Accordingly, after completion of a process of forming the oxide film, the oxide film formed on the front surface must be removed.

An oxide film formed on the front surface is generally removed by polishing. However, since the polishing speed of an oxide film is much slower than the polishing speed of a silicon, it takes a very long time to polish off a thermal oxide film which covers the entire front surface of a silicon wafer. Furthermore, uneven polishing is very likely to occur, resulting in a decreased degree of flatness of the silicon wafer. In the case of an atmospheric pressure CVD oxide film, which is formed partially extending onto the front surface, polishing off such an excess portion of the oxide film also causes the degree of the flatness of a silicon wafer to decrease.

In order to avoid these problems, etching off an oxide film only from the front surface while protecting an oxide film on the back surface may be performed. Alternatively, an oxide film may be removed from the front surface by surface grinding, and then the front surface may be polished.

However, these methods require an additional process, resulting in an increased cost of manufacture.

Along with a recent tendency to increase the degree of integration and precision of semiconductor devices, there has been an increasing demand for silicon wafers having a diameter of not less than 200 mm. When an epitaxial layer is to be grown on a silicon wafer having a large diameter of not less than 200 mm, a low temperature epitaxial growth process is applied in order to obtain a uniform thickness and a uniform resistivity distribution in an epitaxial layer, to reduce a transition width (the width of a region which is located in the vicinity of the boundary between an epitaxial layer and a silicon wafer, each having a different dopant concentration, and in which a dopant concentration transits), to reduce contamination with metal atoms, etc. In order to obtain such a quality, a wafer subjected to a low temperature epitaxial growth process is required to further improve its degree of flatness and reduce its warpage as compared with a wafer to be subjected to a conventional high temperature epitaxial growth process.

However, as mentioned previously, when an atmospheric pressure CVD oxide film or a thermal oxide film is used as a protective film formed on the back surface of a silicon wafer, the degree of flatness of a front surface deteriorates, and a relatively large stress acts on the silicon wafer, resulting in an increased warpage of the silicon wafer. This effect is particularly noticeable with a silicon wafer having a large diameter. Therefore, there

arises a problem when such a wafer is subjected to a photolithographic process, which strictly requires a high degree of flatness. Further, too large a stress causes crystal defects in a wafer.

A layer formed on the back surface of a silicon wafer is also utilized as a gettering layer for gettering heavy metal and the like.

Gettering is a technique for collecting impurities, such as heavy metal, which are generated in the course of manufacturing semiconductor devices from a silicon wafer, to outside of a device region on the front surface of a silicon wafer, thereby preventing device characteristics from degradation.

According to a typical gettering method, polycrystalline silicone is deposited on the back surface of a silicon wafer to form a gettering layer. In order to deposit polycrystalline silicone so as to form a gettering layer, a low pressure CVD method is usually carried out. However, the growth of polycrystalline silicon causes stress to act on a wafer, resulting in a larger warpage of the wafer as compared with a wafer having no polycrystalline silicon layer. Also the warpage of a wafer increases when the diameter of the wafer increases if a polycrystalline silicon layer is grown in a same condition.

Also, as a wafer having a polycrystalline silicon layer is subjected to heat treatment in the course of the fabrication of devices the polycrystalline silicon is gradually crystallized into monocrystal. resulting in a less gettering capability

A silicon wafer utilized from manufacturing semiconductor devices is required to have and maintain a gettering capability during the manufacture of semiconductor devices. In this connection. there is a problem that the warpage of a wafer increases with the diameter of the wafer.

In order to improve a gettering capability, in a silicon wafer having a polycrystalline silicon layer as a gettering layer on the back surface thereof, a stress acting on the wafer must be increased. Therefore. an improvement in the gettering capability and a reduction in stress, i.e. a reduction in warpage, cannot be achieved simultaneously. Furthermore, as heat treatment progresses during the manufacture of semiconductor devices, a polycrystalline silicon layer is gradually crystallized into monocrystal, resulting in difficulty in maintaining the gettering capability.

When an epitaxial layer is to be formed on a silicon wafer having a low dopant concentration, formation of a gettering layer on the back surface of the wafer is sufficient because there is no problem of autodoping. However, when a silicon wafer having a high dopant concentration is used, a protective film which has both a gettering capability and an autodoping preventive capability must be formed on the back surface of the wafer.

However, when a polycrystalline silicon layer is formed on a back surface of a silicon wafer having a high dopant concentration, a gettering effect is obtained, but an autodoping preventive capability is not obtained, since a dopant released from the silicon wafer readily diffuses through the polycrystalline silicon layer.

When an atmospheric pressure CVD oxide film is formed on a silicon wafer, an effect that prevents autodoping is obtained, and a gettering effect is also obtained since a stress acts between the silicon wafer and the oxide film. However, due to difficulty in controlling the stress, the warpage of the silicon wafer tends to be increased.

SUMMARY OF THE INVENTION

This invention has been accomplished in view of the above-mentioned problems, and it is an object of the present invention to provide an improved semiconductor wafer having an autodoping preventive film, in which even when the semiconductor wafer has a large diameter of not less than 200 mm, the stress acting to the wafer and resultant warpage of the wafer can be decreased while maintaining a uniform thickness distribution, a uniform resistivity distribution and a narrow transition width of an epitaxial layer grown on the semiconductor wafer, and in which the front surface of the semiconductor wafer can have an excellent degree of flatness without requiring an extra process such as a process of etching off an oxide film from the front surface.

Another object of the present invention is to provide a semiconductor wafer which has an excellently persistent gettering capability, an autodoping preventive capability and a small stress acting thereon with a resultant small warpage thereof.

A further object of the present invention is to provide a semiconductor epitaxial wafer comprising the above-described semiconductor wafer and an epitaxial layer grown thereon, and a method of manufacturing the same.

According to an aspect of the present invention, there are provided:

1) a method of manufacturing a semiconductor wafer which has a dopant evaporation preventive film formed on one of main surfaces thereof, wherein a film serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method;

2) a method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is formed on one of main surfaces and a semiconductor thin film is formed on the other main surface by epitaxial growth, wherein a film serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, and the semiconductor wafer is subject to heat treatment at a temperature lower than a temperature at which the epitaxial growth of the semiconductor thin film is carried out;

3) a method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is

formed on one of main surfaces, wherein in that a film serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, and the other main surface is then polished; and

4) a method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is formed on one of main surfaces and a semiconductor thin film is formed on the other main surface by epitaxial growth, wherein a film serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, the semiconductor wafer is subject to heat treatment at a temperature lower than a temperature at which the expitaxial growth of the semiconductor thin film is carried out, and the other main surface is then polished.

Preferably, the dopant evaporation preventive film is selected from a group consisting of silicon oxide film, silicon nitride film and silicon oxynitride film.

Preferably, the dopant evaporation preventive film is formed such that a stress between the dopant evaporation preventive film and the semiconductor wafer becomes equal to or less than $1x10^7$ dyne/cm^2.

According to the above-described aspect of the present invention, it is possible to provide a semiconductor wafer having a dopant evaporation preventive film on the back surface of the wafer, in which the stress acting to the wafer and resultant warpage of the wafer can be decreased even when the wafer has a large diameter, while maintaining a uniform thickness distribution, a uniform resistivity distribution and a narrow transition width of an epitaxial layer grown on the semiconductor wafer, and in which the front surface of the semiconductor wafer can have an excellent flatness without requiring an extra process.

Another aspect of the present invention, there are provided the following methods of manufacturing a semiconductor wafer:

5) a method of manufacturing a semiconductor wafer having a plasma CVD film on one of main surfaces, wherein the plasma CVD film is formed on the one of the main surfaces of the semiconductor wafer so that a stress between the plasma CVD film and the semiconductor wafer falls in a range of 1×10^8 - 1×10^9 dyne/cm^2; and

6) a method of manufacturing a semiconductor wafer having a plasma CVD film on one of main surfaces, wherein the plasma CVD film is formed on the one of the main surfaces of the semiconductor wafer, and the semiconductor wafer is then subjected to heat treatment so that a stress between the plasma CVD film and the semiconductor wafer falls in a range of 1×10^8 - 1×10^9 dyne/cm^2.

The other main surface of the semiconductor wafer on which the plasma CVD film has not been formed is generally polished after the formation of the plasma CVD film or after the heat treatment of the semiconductor wafer. In the method of the present aspect, however, the plasma CVD film may be formed on the one of the main surfaces after the other main surface has been mirror-polished.

Preferably, the plasma CVD film is selected from a group consisting of silicon oxide film, silicon nitride film and silicon oxynitride film, because these films have excellent autodoping preventing effects, and their source gases are generally available.

According to the aspect of the present invention, it is possible to provide a semiconductor wafer which has an excellently persistent gettering capability and an autodoping preventive capability and a small stress acting thereon with a resultant small warpage thereof.

According to another aspect of the present invention, there are provided a semiconductor wafer manufactured by one of the above-described method, and a semiconductor epitaxial wafer manufactured by one of the above-described method in which a semiconductor thin film is formed by epitaxial growth, on the other main surface of the semiconductor wafer on which the plasma CVD film is not formed.

According to still another aspect of the present invention, there is provided a method of manufacturing a semiconductor epitaxial wafer, wherein a plasma CVD film is formed on one of main surfaces of a semiconductor wafer, and a semiconductor thin film is formed by epitaxial growth, on the other main surface on which the plasma CVD film is not formed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A - 1C are schematic diagrams showing a method of manufacturing a semiconductor wafer according to the present invention;

FIG. 1D is a schematic diagram showing an epitaxial wafer manufactured using the semiconductor wafer shown in FIG. 1C;

FIGS. 2A - 2D are schematic diagram showing another method of manufacturing a semiconductor wafer according to the present invention, wherein the portion above a broken line in FIG. 2D indicates a portion to be removed by mirror polishing; and

FIGS. 3A - 3D are schematic diagram showing a method of manufacturing a silicon epitaxial wafer according to the present invention, wherein the portion above a broken line in FIG. 3C indicates a portion to be removed by mirror polishing.

DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention will now be described with reference to the drawings.

First Embodiment:

First, a semiconductor wafer 1 manufactured by a known method is prepared as shown in FIG. 1A. For this semiconductor wafer, a chemically-etched wafer that has not yet been subjected to mirror-polishing is normally used, but a polished wafer having one or both of the main surfaces thereof mirror polished.

Subsequently, as shown in FIG. 1B, a plasma CVD film 2 is deposited on one of the main surfaces of the thus-prepared semiconductor wafer by using a parallel-plate-type plasma CVD system. Although the kind of plasma CVD film to be deposited on the wafer is not limited, silicon oxide film, silicon nitride film or silicon oxynitride film is suitable because these films can be formed by using gases of generally avairable.

The deposition conditions are controlled such that the deposition temperature falls within the range of 300 - 450°C, the deposition pressure falls within the range of 1 - 10 torr, and the deposition film thickness falls within the range of 100 - 500 nm, and so that the stress of the plasma CVD film applied to the semiconductor wafer preferably becomes equal to or less than 1×10^7 dyne/cm^2. The magnitude of the stress can be measured in a non-destructive manner by use of a commercially available laser Raman spectrophotometer, which projects a laser beam onto the plasma CVD film.

After the deposition of the plasma CVD film, as shown in FIG. 1C, the other main surface opposite to the surface on which the plasma CVD has been deposited is mirror-polished, whereby a desired semiconductor wafer having an autodoping preventive film can be obtained. Since the plasma CVD film deposited on the surface can be polished off at a much higher speed as compared to the case where a thermal oxide film or an atmospheric pressure CVD oxide film is polished, the plasma CVD film can be easily removed by mirror polishing. Consequently, the flatness of the semiconductor wafer can be maintained.

In the case where the surface opposite to the surface on which a plasma CVD film is to be deposited has been mirror-finished, a subsequent polishing process can be omitted if the plasma CVD is prevented from depositing on the mirror-finished surface.

Moreover, as shown in FIG. 1D, an epitaxial layer 3 is grown on the semiconductor wafer obtained through the above-described steps, at a low temperature equal to or less than 1000°C and by use of a commercially available epitaxial reactor, so that a desired epitaxial wafer with a slight warpage can be obtained.

When the wafer on which the plasma CVD has been deposited is heat treated, before the mirror-polishing step, at a temperature lower than the temperature of the subsequently-performed epitaxial growth, the plasma CVD film is baked and hardened, so that a protective film having a higher autodoping preventive capability can be obtained. The reason why the heat treatment temperature is set to a temperature lower than the epitaxial growth temperature is to reduce the stress caused by the hardened plasma CVD film onto the semiconductor wafer.

Example 1:

Three kinds of silicon wafers were prepared from a silicon ingot manufactured by the Czochralski method (each wafer had a diameter of 200 mm, a {100} main surface, a thickness of 750 μm, a p-type conductivity, and a resistivity of 0.01 Ω·cm). Plasma CVD films (either silicon oxide film, silicon nitride film or silicon oxynitride film) were deposited on each of the first main surface of the wafers by use of a plasma CVD reactor using radio-frequency of 13.56 MHz (Concept-One, product of Novellus Systems Inc.).

When a silicon oxide film was formed as a plasma CVD film, monosilane and nitrous oxide were supplied as source materials to a plasma reaction chamber while nitrogen was used as a carrier gas, and the silicon oxide film was deposited until its thickness reached 500 nm at a growth temperature of 425°C and a growth pressure of 3 torr. At this time, a high frequency power of 700 W was supplied to an upper plate located above a wafer in the plasma reaction chamber, while a low frequency power of 300 W was supplied to a lower plate located below the wafer, so that the stress of the silicon oxide film applied to the wafer became equal to or less than 1×10^7 dyne/cm^2.

When a silicon nitride film was formed as a plasma CVD film, monosilane and ammonia were used as source materials. The formation of the silicon nitride film was carried out under the same conditions as for the silicon oxide film until the thickness reached 100 nm so that the stress of the silicon nitride film applied to the wafer became equal to or less than 1×10^7 dyne/cm^2.

When a silicon oxynitride film was formed as a plasma CVD film, monosilane, nitrous oxide, and ammonia were used as source materials. The formation of the silicon oxynitride film was carried out under the same conditions as for the silicon oxide film until the thickness reached 300 nm so that the stress of the silicon oxynitride film applied to the wafer became equal to or less than 1×10^7 dyne/cm^2.

The thus-obtained wafers of the three kinds were observed to have little warpage when the stress acting thereon was equal to or less than 1×10^7 dyne/cm^2.

Subsequently, the second surface of each wafer opposite to the first surface on which the plasma CVD was deposited was polished, and an epitaxial film having a thickness of 4 μm was grown at low-temperature of 800°C. In each of the cases where any kinds of the plasma CVD films above-mentioned were formed, the resistivity distribution of the silicon epitaxial layer within the wafer surface was equal to or less than ±5%. The transition width of the silicon epitaxial layer became equal to or less than the half of that of an epitaxial layer deposited at 1100°C. This occurred because dopant in the

silicon wafer was prevented from evaporating at the back surface of the wafer not to cause autodoping, and the sold-phase diffusion of the dopant into the epitaxial layer was decreased. The amount of an increase in the warpage of the wafer after the formation of the epitaxial layer compared to the warpage before the formation of the epitaxial layer was as low as 5 μm or less.

The resistivity was measured at nine points within the wafer surface, and the resistivity distribution was calculated in accordance with the following equation:

$$\text{Resistivity distribution (\%)} = \pm(M-m)/(M+m)$$

where M is the maximum value of the measured resistivity, and m is the minimum value of the measured resistivity.

Second Embodiment:

First, a semiconductor wafer 4 manufactured by a known method is prepared as shown in FIG. 2A. For this semiconductor wafer, a chemically-etched wafer that has not yet been subjected to mirror-polishing is generally used. However, a polished wafer having one main surface or both main surfaces thereof mirror polished may be used.

Subsequently, as shown in FIG. 2B, a plasma CVD film 5 is deposited on one of main surfaces of the thus-prepared semiconductor wafer by use of a parallel-plate-type plasma CVD reactor so that the stress of the plasma CVD film applied to the semiconductor wafer falls within a range of 1×10^8-1×10^9 dyne/cm^2.

The reason why the plasma CVD film 5 is deposited so that the stress acting to the semiconductor wafer falls within the range of 1×10^8 - 1×10^9 dyne/cm^2 is that such stress creates strained layer which captures impurities such as metals, thereby serving as a gettering layer. When the stress is less than 1×10^8 dyne/cm^2, sufficient gettering capability cannot be obtained. When the stress is greater than 1×10^9 dyne/cm^2, the warpage of the wafer increases. The magnitude of the stress can be measured in a non-destructive manner by use of a commercially available laser Raman spectrophotometer, which projects a laser beam onto the plasma CVD film.

Although there is no limitation on the kind of plasma CVD film to be deposited on the wafer, silicon oxide film, silicon nitride film or silicon oxynitride film is suitable because these films have an autodoping preventive capability and can be formed by use of generally available gasses.

The deposition of the plasma CVD film is usually performed such that the deposition temperature falls within a range of 300 - 450°C, the deposition pressure falls within a range of 1 - 10 torr, and the deposition film thickness falls within a range of 100 - 500 nm. Within these ranges, the deposition conditions are controlled so that the stress which the plasma CVD film applies to the semiconductor wafer falls within a range of 1×10^8 - 1×10^9 dyne/cm^2.

Alternatively, after the deposition of the plasma CVD film 2, the silicon wafer may be subjected to heat treatment so that the stress acting between the plasma CVD film and the semiconductor wafer falls within a range of 1×10^8 - 1×10^9 dyne/cm^2, thereby forming a strained layer 6 as shown in FIG. 2C.

Even when the thus-formed plasma CVD film undergoes heat treatment during fabrication of semiconductor devices, the stress acting to the semiconductor wafer does not decrease but rather increase slightly, so that the gettering capability does not decrease.

After the deposition of the plasma CVD film or after heat treatment, the other main surface opposite to the main surface on which the plasma CVD has been deposited is mirror-polished, whereby there can be obtained a desired semiconductor wafer which has an excellently persistent gettering capability, an autodoping preventive capability and small stress acting to the wafer with a resultant small warpage thereof (see FIG. 2D). Since the plasma CVD film deposited on the surface can be polished off at much higher speed as compared to the case where a thermal oxide film or an atmospheric pressure CVD oxide film is polished, the plasma CVD film can be easily removed by mirror polishing. Consequently, the flatness of the semiconductor wafer can be maintained.

In the case where the surface opposite to the surface on which a plasma CVD film is to be deposited has been mirror-finished, a subsequent polishing process can be omitted if the plasma CVD is prevented from depositing on the mirror-finished surface.

Moreover, an epitaxial layer may be grown on the semiconductor wafer obtained through the above-described steps by use of a commercially available epitaxial reactor, so that there can be obtained a desired epitaxial wafer which has an excellently persistent gettering capability, an autodoping preventive capability, and a small stress acting to the wafer with a resultant small warpage thereof.

The epitaxial growth process may be used as a replacement of heat treatment given to the semiconductor wafer on which the plasma CVD film is deposited. That is, a semiconductor wafer 4 is prepared as shown in FIG. 3A, and a plasma CVD film 5 is deposited on the first main surface of the semiconductor wafer 4, as shown in FIG. 3B. Subsequently, the second main surface of the semiconductor wafer 4 opposite the first main surface on which the plasma CVD film 5 has been deposited is mirror polished, as shown in FIG. 3C. After that, an epitaxial layer 7 is grown on the mirror-polished second main surface. The epitaxial growth is conducted at a temperature in a range of 800 - 1200°, whereby the stress which the plasma CVD film applies to the semiconductor wafer falls within a range of 1×10^8 - 1×10^9 dyne/cm^2. As a result, the portions that receive the stress form a strained layer 6, as shown in FIG. 3D.

Example 2:

Four kinds of silicon wafers were prepared from a silicon ingot manufactured by the Czochralski method (each wafer had a diameter of 150 mm, a {100} main surface, a thickness of 630 μm, a p-type conductivity, and a resistivity of 0.01Ω·cm). Silicon oxide film, silicon nitride film or silicon oxynitride film were respectively deposited, as a plasma CVD film, on the first main surfaces of three kinds of wafers by use of a plasma CVD reactor using radio-frequency of 13.56 MHz(Concept-One, product of Novellus Systems Inc.). The remaining one kind of wafer was used as it was without forming the plasma CVD film.

When a silicon oxide film was formed as a plasma CVD film, monosilane and nitrous oxide were supplied as source materials to a plasma reaction chamber while nitrogen was used as a carrier gas, and the silicon oxide film was deposited until its thickness reached 500 nm at a growth temperature of 425°C and a growth pressure of 3 torr. At this time, a high frequency power of 700 W was supplied to an upper plate located above a wafer in the plasma reaction chamber, while a low frequency power of 300 W was supplied to a lower plate located below the wafer, so that the stress of the silicon oxide film applied to the wafer became equal to 1×10^8 dyne/cm^2.

When a silicon nitride film was formed as a plasma CVD film, monosilane and ammonia were used as source materials. The formation of the silicon nitride film was carried out under the same conditions as for the silicon oxide film until the thickness reached 100 nm so that the stress of the silicon nitride film applied to the wafer became equal to 1×10^8 dyne/cm^2.

When a silicon oxynitride film was formed as a plasma CVD film, monosilane, nitrous oxide and ammonia were used as source materials. The formation of the silicon oxynitride film was carried out under the same conditions as for the silicon oxide film until the thickness reached 300 nm so that the stress of the silicon oxynitride film applied to the wafer became equal to 1×10^8 dyne/cm^2.

The thus-obtained wafers of three kinds had warpages not greater than 3 μm when the stress acting thereon was 1×10^8 dyne/cm^2.

Subsequently, the second surface of each wafer opposite to the first surface on which the plasma CVD was deposited was polished, and an epitaxial film having a thickness of 5 μm was grown at 1100°C. In each of the cases where any kinds of the plasma CVD films abovementioned were formed, the resistivity distribution of the silicon epitaxial layer within the wafer surface was equal to or less than ±5%. The transition width of the silicon epitaxial layer became about half of that of an epitaxial layer deposited on a wafer having no plasma CVD film.

The resistivity was measured at nine points within the wafer surface, and the resistivity distribution was calculated in accordance with the following equation:

Resistivity distribution (%) = ±(M-m) / (M+m)

where M is the maximum value of the measured resistivity, and m is the minimum value of the measured resistivity.

Measurement about the gettering capability was performed as follows. An iron-containing solution was applied to the surface of each of four kinds of wafers that were manufactured under the same conditions as above-described, so that the thus-coated surface of each silicon wafer was intentionally contaminated. Thereafter, the silicon wafers were subjected to heat treatment at a temperature of 1000°C for one hour, so that iron was diffused into the silicon wafers. Subsequently, the silicon wafers were further subjected to heat treatment at a temperature of 650°C for ten hours. Then, the concentration of iron in each silicon wafer with exclusion of the plasma CVD film was measured.

By using the concentration of iron in the silicon wafer having no plasma CVD film as a reference, a ratio of iron captured by the plasma CVD film was calculated from a measurement value of the iron concentration. Thus-calculated ratio was used as a gettering capability. The results revealed that the gettering capability of the semiconductor wafer on which a plasma CVD film was formed according to the present invention was 93 - 96%.

As is evident from the test result, the semiconductor wafer on which a plasma CVD film was formed according to the present invention had an excellently persistent gettering capability and an autodoping preventive capability.

Moreover, the amount of an increase in the warpage of the wafer after the formation of the epitaxial layer compared to the warpage before the formation of the epitaxial layer was as low as 5 μm or less. This demonstrates that the semiconductor wafer on which a plasma CVD film was formed according to the present invention had a reduced warpage.

The present invention is not limited to the above-described embodiment. The above-described embodiment is a mere example, and those having the substantially same structure as that described in the appended claims and providing the similar action and effects are included in the scope of the present invention.

Claims

1. A method of manufacturing a semiconductor wafer which has a dopant evaporation preventive film formed on one of main surfaces thereof, characterized in that a plasma CVD film 2 serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method.

2. A method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is

formed on one of main surfaces and a semiconductor thin film is formed on the other main surface by epitaxial growth, characterized in that a plasma CVD film 2 serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, and the semiconductor wafer is subject to heat treatment at a temperature lower than a temperature at which the expitaxial growth of the semiconductor thin film is carried out.

3. A method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is formed on one of main surfaces, characterized in that a plasma CVD film 2 serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, and the other main surface is then polished.

4. A method of manufacturing a semiconductor wafer in which a dopant evaporation preventive film is formed on one of the main surfaces and a semiconductor thin film is formed on the other main surface by epitaxial growth, characterized in that a plasma CVD film 5 serving as the dopant evaporation preventive film is formed on the one of the main surfaces by a plasma CVD method, the semiconductor wafer is subject to heat treatment at a temperature lower than a temperature at which the expitaxial growth of the semiconductor thin film 7 is carried out, and the other main surface is then polished.

5. A method of manufacturing a semiconductor wafer according to any one of Claims 1 - 4, characterized in that the plasma CVD film 5 is formed so that a stress between the plasma CVD film 5 and the semiconductor wafer 4 becomes equal to or less than 1×10^7 dyne/cm^2.

6. A method of manufacturing a semiconductor wafer having a plasma CVD film 5 on one of main surfaces, characterized in that the plasma CVD film 5 is formed on the one of the main surface of the semiconductor wafer 4 so that a stress between the plasma CVD film 5 and the semiconductor wafer 4 falls in a range of 1×10^8 - 1×10^9 dyne/cm^2.

7. A method of manufacturing a semiconductor wafer according to Claim 6, characterized in that the other main surface of the semiconductor wafer 4 on which the plasma CVD film 5 has not been formed is polished after the formation of the plasma CVD film 5.

8. A method of manufacturing a semiconductor wafer according to Claim 6, characterized in that the plasma CVD film 5 is formed on one of main surfaces of the wafer 4 after at least the other main surface has been mirror-polished.

9. A method of manufacturing a semiconductor wafer having a plasma CVD film on one of main surfaces, characterized in that the plasma CVD film 5 is formed on the one of the main surfaces of the semiconductor wafer 4, and the semiconductor wafer is then subjected to heat treatment so that a stress between the plasma CVD film 5 and the semiconductor wafer 4 falls in a range of 1×10^8 - 1×10^9 dyne/cm^2.

10. A method of manufacturing a semiconductor wafer according to Claim 9, characterized in that the other main surface of the semiconductor wafer 4 on which the plasma CVD film 5 has not been formed is polished after the semiconductor wafer is subjected to heat treatment.

11. A method of manufacturing a semiconductor wafer according to Claim 9, characterized in that the plasma CVD film 5 is formed on one of the main surfaces of the wafer after at least the other main surface has been mirror-polished.

12. A method of manufacturing a semiconductor wafer according to any one of Claims 1 -11, characterized in that the plasma CVD film 5 is selected from a group consisting of silicon oxide film, silicon nitride film, and silicon oxynitride film.

13. A semiconductor wafer manufactured by the method described in any one of Claims 1 - 11.

14. A semiconductor epitaxial wafer in which a semiconductor thin film 7 is formed by epitaxial growth, on one of main surfaces of the semiconductor wafer 4 manufactured by the method described in any one of Claims 1 - 11, wherein the plasma CVD film 5 is not formed on the one of the main surfaces.

15. A method of manufacturing a semiconductor epitaxial wafer, characterized in that a plasma CVD film 5 is formed on one of main surfaces of a semiconductor wafer, and a semiconductor thin film 7 is formed by epitaxial growth, on the other main surface on which the plasma CVD film 5 is not formed.

FIG. IA

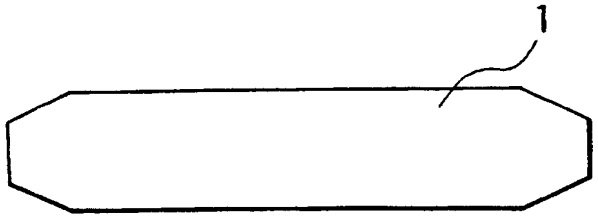


FIG. IB

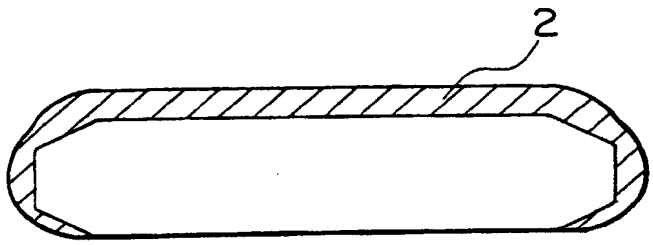


FIG. IC

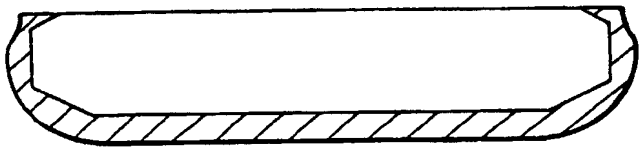


FIG. ID

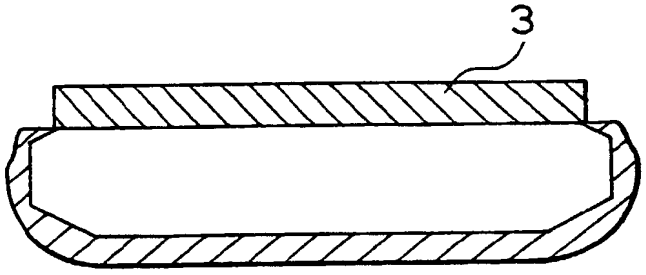


FIG. 2A

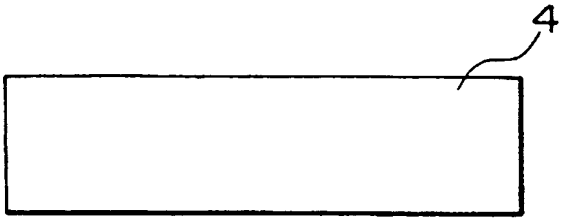


FIG. 2B

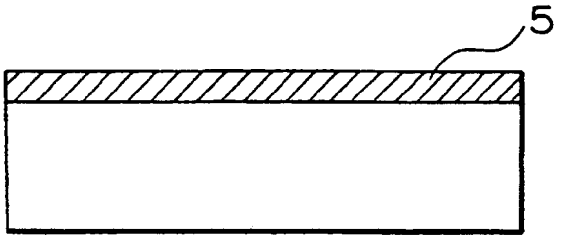


FIG. 2C

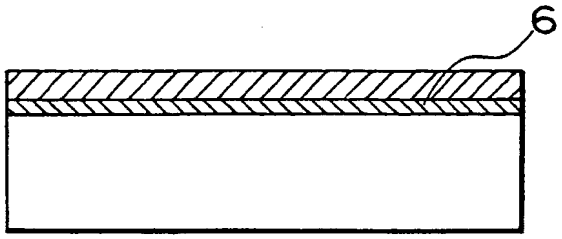


FIG. 2D

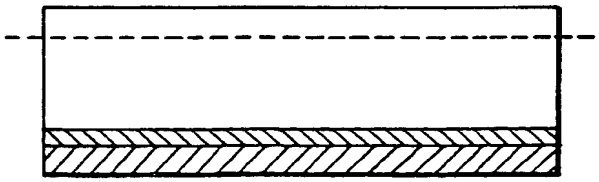


FIG. 3A

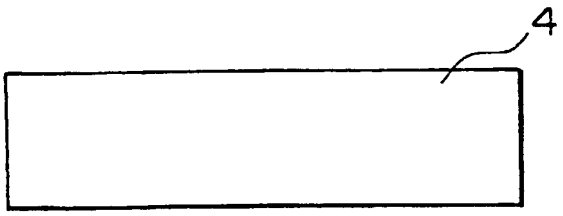


FIG. 3B

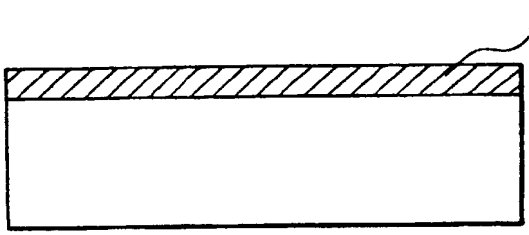


FIG. 3C

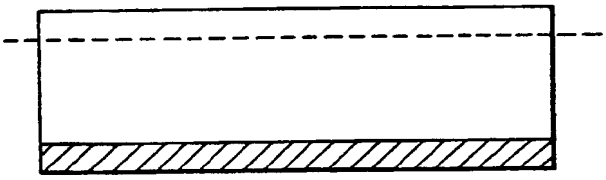
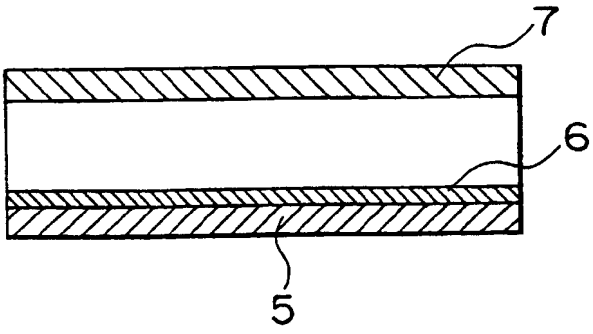


FIG. 3D



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28.03.1996 JP 99369/96

(71) Applicant **SHIN-ETSU HANDOTAI COMPANY LIMITED**
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(54) **Method of manufacturing a semiconductor wafer comprising a dopant evaporation preventive film on one main surface and an epitaxial layer on the other main surface**

(57) There is disclosed a method of manufacturing a semiconductor wafer which has a dopant evaporation preventive film formed on one of the main surfaces thereof by a plasma CVD method. There is also disclosed a method of manufacturing a semiconductor wafer having a plasma CVD film on one of main surfaces, wherein the plasma CVD film is formed on the one of the main surfaces of the semiconductor wafer so that a stress between the plasma CVD film and the semiconductor wafer falls in a range of 1×10^8 - 1×10^9 dyne/cm^2.

FIG. 1A

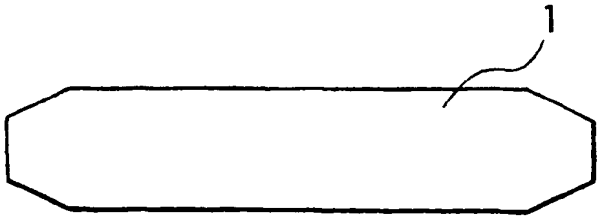

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FIG. 1B

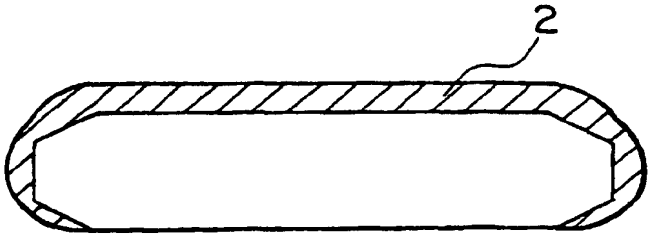


FIG. 1C

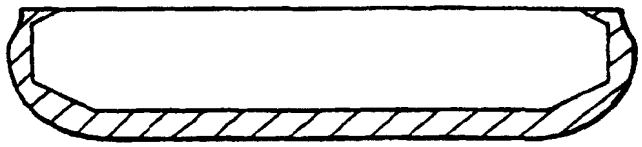
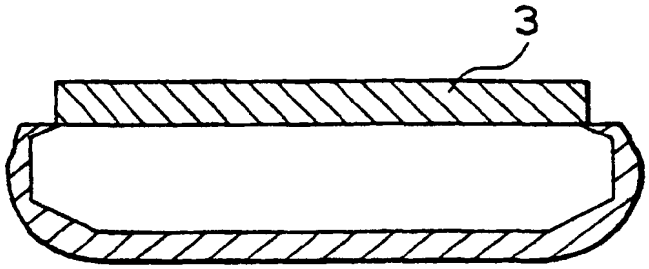


FIG. 1D



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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 2067

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 489 (E-696), 21 December 1988 & JP 63 204732 A (NEC CORP), 24 August 1988, * abstract *	1,12,13	H01L21/322 H01L21/22 H01L21/20 H01L21/324 H01L21/304 H01L21/314 H01L21/316 C30B25/00
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A		2,4,14, 15	

Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 380 (E-0965), 16 August 1990 -& JP 02 138738 A (FUJI ELECTRIC CO LTD), 28 May 1990, * abstract *	5	
A		1-4, 12-15	

X	US 5 296 385 A (MOSLEHI MEHRDAD M ET AL) 22 March 1994 * column 1, line 44 - line 56 * * column 2, line 1 - line 46; figure 5 *	1,12,13	
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Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 111 (E-246), 24 May 1984 & JP 59 027529 A (CLARION KK), 14 February 1984, * abstract *	3	H01L C30B
A		1,5,12, 13	

X	PATENT ABSTRACTS OF JAPAN vol. 005, no. 137 (E-072), 29 August 1981 -& JP 56 071928 A (CHIYOU LSI GIJUTSU KENKYU KUMIAI), 15 June 1981, * abstract *	14	
Y		2,4,15	

	-/--		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	11 May 1998	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

Application Number
EP 97 30 2067

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

SEE SHEET B
(in case of Lack of Unity)

☐ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☒ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

1-5 12-15

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 2067

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 437 (E-0980), 19 September 1990 & JP 02 170430 A (FUJI ELECTRIC CO LTD), 2 July 1990, * abstract *	2,4,15	
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 479 (E-0992), 18 October 1990 & JP 02 197128 A (SHIN ETSU HANDOTAI CO LTD), 3 August 1990, * abstract *	14	
Y		4	
A		2,15	
X	PATENT ABSTRACTS OF JAPAN vol. 013, no. 584 (E-866), 22 December 1989 & JP 01 246822 A (SHIN ETSU HANDOTAI CO LTD), 2 October 1989, * abstract *	14	
A		2,4,15	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 007, no. 194 (E-195), 24 August 1983 & JP 58 095819 A (TOKYO SHIBAURA DENKI KK), 7 June 1983, * abstract *	14	
A		2,4,15	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	11 May 1998	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

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& : member of the same patent family, corresponding document

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European Patent Office

LACK OF UNITY OF INVENTION
SHEET B

Application Number
EP 97 30 2067

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: Claims 1, 3, 5, 12, 13

   A method of manufacturing a semiconductor wafer with a step of forming a dopant evaporation preventing film by plasma CVD on one of the main surfaces of said wafer, and semiconductor wafer thereby formed.

2. Claims: Claims 2, 4, 14, 15

   A method of manufacturing a semiconductor wafer with a step of forming a film by plasma CVD on one of the main surfaces of said wafer and a step of epitaxially growing a semiconductor thin film on the other main surface with further steps of heating, polishing, and semiconductor "epitaxial wafer" thereby formed (in claims 2, 4, the film is a dopant evaporation preventing film).

3. Claims: Claim 6-11

   A method of manufacturing a semiconductor wafer with a step of forming a film by plasma CVD on one of the main surfaces of said wafer with a stress between the film and the wafer falling in a range of 10E8 - 10E9 dyne/cm2.

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EUROPEAN SEARCH REPORT

Application Number
EP 97 30 2067

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 4 925 809 A (YOSHIHARU TETSUJIRO ET AL) 15 May 1990 * column 1, line 17 - column 2, line 25; figures 1,2 * * column 2, line 52 - line 60 * * column 3, line 30 - column 4, line 25; figure 6 * * column 4, line 60 - column 5, line 11; figures 5,9 *	14	
A		2,4,15	
P,X	US 5 562 770 A (CHEN BOMY A ET AL) 8 October 1996 * column 1, line 5 - line 9 * * column 2, line 15 - line 35 * * column 5, line 40 - column 6, line 21; figure 7 *	16	
P,A		1,2,15	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	11 May 1998	Klopfenstein, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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& : member of the same patent family, corresponding document

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